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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,314	10/16/2003	Yi-Hsun Wu	24061.27 / TSMC2002-1168	7810

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/687,314	WU ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,8-10 and 12-17* is/are allowed.

6)☒ Claim(s) *1,2,4-7,11,18-21 and 23* is/are rejected.

7)☒ Claim(s) *22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-7 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishita. As to claim 1, Morishita, Figure 4, discloses a deep submicron electrostatic discharge (ESD) protection structure comprising first and second electrodes (S3) and (S4), separated by an ultra thin oxide material (3), a silicide (S6) covered, grounded gate (4) positioned above the ultra thin oxide material, a source (ND2) positioned proximate to the first electrode, and a drain (ND3) positioned proximate to the second electrode and covered by a silicide layer (S4), wherein the silicide layer enhances ESD protection provided by the structure.

As to claim 2, Morishita, paragraph [0098] discloses that the ultra thin oxide material comprises a thin oxide layer 19 Å in thickness.

As to claim 4, Morishita, paragraph [0054] discloses that the silicide layer, including (S6) is a metal silicide layer.

As to claim 5, Morishita, paragraph [0054] expressly discloses that the metal silicide may by cobalt silicide or titanium silicide.

As to claim 6, Morishita, paragraph [0054] discloses the formation of an n-channel metal oxide FET.

As to claim 7, the conductivity types of all components in a semiconductor device may be interchanged between n-type and p-type.

As to claim 11, Morishita, paragraph [0057] discloses that the structure is associated with a transition time from breakdown to snapback, wherein the silicide layer shortens the transition time.

Claims 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishita. As to claim 18, Morishita, Figure 4, discloses a method for fabricating a deep submicron electrostatic discharge (ESD) protection structure comprising forming a well region (2), forming a thin gate oxide (3) layer above the well region, forming a silicide covered, grounded polysilicon gate structure (4) and (S6) above the gate oxide layer, forming a source region (ND2) proximate to the gate oxide layer, forming a drain region (ND3) proximate to the gate oxide layer and opposite the source region, and forming a silicide layer (S3) and (S4) over the drain region.

As to claim 19, Morishita, paragraph [0098] discloses that the ultra thin oxide material comprises a thin oxide layer 19 Å in thickness.

As to claim 20, Morishita, paragraph [0054] expressly discloses that the metal silicide may by cobalt silicide or titanium silicide.

As to claim 21, Morishita, Figure 4, discloses a silicide region (S3) formed over the source region (ND2).

Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Morishita. Morishita, Figure 4, discloses a deep submicron electrostatic discharge (ESD) protection structure comprising an n-channel metal oxide semiconductor having a thin oxide layer (3) formed on the substrate, a silicide covered, grounded gate (4) and (S6) positioned on the thin oxide layer, a silicide covered source (ND2) and (S3) positioned proximate to the thin oxide layer on one side of the grounded gate, and a silicide covered drain (ND3) and (S4) positioned proximate to the thin oxide layer on the side of the grounded gate opposite the source.

Allowable Subject Matter

Claims 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 8-10, 12-17 are allowed. Morishita, nor any other prior art has the claimed channel dimensions or a floating drain.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
January 7, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800